Appendice G

Acronimi

ADC *Analog Digital Converter*

ARQ *Automatic ReQuest for repeat*

BER *Bit Error Rate*

BPSK *Binary Phase Shift Keying*

CIC *Cascaded Integrator Comb*

CLB *Configurable Logic Block*

CORDIC *COordinate Rotate DIgital Computer*

CPFSK *Continuous Phase Frequency Shift Keying*

CPLD *Complex Programmable Logic Device*

DAC *Digital Analog Converter*

DDS *Direct Digital Synthesizer*

DDFS *Direct Digital Frequency Synthesizer*

DLL *Delay Locked Loop*

DSP *Digital Signal Processing*

FA *Full Adder*

FEC *Forward Error Correction*

FFD *Flip Flop D*

FIFO *First In First Out*

FPGA *Field Programmable Gate Array*

FSK *Frequency Shift Keying*

GMSK *Gaussian Minimum Shift Keying*

GRM *General Routing Matrix*

IDFT *Inverse Discrete Fourier Transform*

IF *Intermediate Frequency*

IOB *Input Output Block*

ISI *Inter Symbol Interference*

ISP *In System Programmable*

LC *Logic Cell*

LUT *Look-Up Table*

MAP *Maximum A Posteriori probability*

ML *Maximum Likelihood*

MSB *Most Significant Bit*

MSK *Minimum Shift Keying*

NCO *Numerical Control Oscillator*

NRZ *No Return to Zero*

OQPSK *Offset Quadrature Phase Shift Keying*

OTP *One Time Programmable*

PAL *Programmable Array Logic*

PAR *Place And Route*

PCF *Physical Constrain File*

PLD *Programmable Logic Device*

PSK *Phase Shift Keying*

QAM *Quadrature Amplitude Modulation*

QPSK *Quadrature Phase Shift Keying*

RAM *Random Access Memory*

RTL *Register Transfer Logic*

SER *Symbol Error Rate*

SFDR *Spurious Free Dynamic Range*

SIPO *Serial In Parallel Out*

SNR *Signal to Noise Ratio*

SRAM *Static Random Access Memory*

SRL16 *Shift Register Left 16-bit*

SRRC *Square Root Raised Cosine*

STA *Static Timing Analyzer*

TWTA *Travelling Wave Tube Amplifier*

UCF *User Constrain File*

VHDL *VHSIC Hardware Description Language*

VHSIC *Very High Speed Integrated Circuit*